12. The semiconductor package of claim 8, wherein the lower wiring pattern extends in at least one direction from the landing pad, and further includes a conductive pattern having a curved line shape.

13. The semiconductor package of claim 12, wherein the conductive pattern has a sine wave shape.

14. The semiconductor package of claim 9, wherein the lower wiring pattern further includes:

a conductive pattern extending from the landing pad in a first direction to be connected to the inner wiring pattern; and

an extended conductive pattern extending from the landing pad in a second direction opposite to the first direction and extending up to an outside region of the trench,

wherein the conductive pattern has a curved line shape.

15. The semiconductor package of claim 2, wherein the interconnection members are disposed to be aligned with the trenches, respectively.

16. The semiconductor package of claim 2, wherein each of the interconnection members includes:

a pillar portion; and

a protrusion portion extending from an end of the pillar portion to have a hemispherical shape,

wherein the protrusion portion is connected to one of the lower wiring patterns.

17. The semiconductor package of claim 16, wherein the protrusion portion of the interconnection member includes a solder material.

18. A semiconductor package comprising:

a first substrate (**200**) having a first surface (**200***a*) and a second surface (**200***b*) facing away from the first surface; and

a second substrate (**231**) disposed over the first surface of the first substrate and haying:

a substrate core (**230**) having a first surface and a second surface facing away from the first surface, wherein a trench (**232***a*) is disposed in the substrate core to be adjacent to the second surface;

an elastic buffer layer (**220**) disposed on the second surface of the substrate core and having an opening (**220***a*) disposed on its surface facing the first substrate, wherein the elastic buffer layer crosses the trench to provide a cavity (S**2**); and

a lower wiring pattern (**250**) disposed inside the elastic buffer layer and having a landing pad (**272**) disposed to be aligned to the trench; and

an interconnection member (**210**) electrically connecting the first substrate to the second substrate, wherein one end of the interconnection member is connected to the lower wiring pattern and the other end is connected to the first substrate.

19. The semiconductor package of claim 18, wherein the second substrate further comprises an outer circuit wiring pattern disposed on the first surface of the second substrate; and

a via electrode penetrating the second substrate from the first surface to the second surface, wherein one of both ends of the via electrode is connected to the outer circuit wiring pattern and the other end is connected to the lower wiring pattern.

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